

REMARKS

The Office Action dated May 18, 2005, has been received and carefully considered. In this response, claims 1, 6, 8, 9, 11, 16, 18-20 have been amended. Entry of the amendments to claims 1, 6, 8, 9, 11, 16, 18-20 is respectfully requested. Reconsideration of the outstanding rejections in the present application is also respectfully requested based on the following remarks.

I. THE ANTICIPATION REJECTION OF CLAIMS 1-10 AND 20

On pages 2-7 of the Office Action, claims 1-10 and 20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Burns et al. (U.S. Patent No. 6,449,291). This rejection is hereby respectfully traversed with amendment.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987).

That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id..

Regarding claim 1, the Examiner asserts that Burns et al. discloses a method for synchronizing clocks in a network, the method comprising: receiving a first timestamp and a second timestamp each indicating a respective time instance within the network; measuring a first time interval between the first timestamp and the second timestamp as determined by a first clock signal; measuring a second time interval between the first timestamp and the second timestamp as determined by a second clock signal; generating a difference signal representing a difference between the first time interval and the second time interval; and generating the second clock signal based upon the difference signal such that the second clock signal is synchronized with the first clock signal.

However, it is respectfully submitted that Burns et al. fails to disclose, or even suggest, a method for synchronizing clocks in a network, the method comprising: receiving a first

timestamp and a second timestamp each indicating a respective time instance within the network; measuring a first time interval between the first timestamp and the second timestamp as determined by a first clock signal; measuring a second time interval between the first timestamp and the second timestamp as determined by a second clock signal; generating a difference signal representing a difference between the first time interval and the second time interval; filtering the difference signal; and generating the second clock signal based upon the filtered difference signal such that the second clock signal is synchronized with the first clock signal, as presently claimed. Indeed, Burns et al. fails to disclose, or even suggest, anything regarding the filtering of a difference signal representing a difference between a first time interval and a second time interval. Despite this deficiency, the Examiner asserts that Burns et al. does disclose filtering of a difference signal in Figure 5, at column 8, lines 40-55, and column 12, lines 14-24 (see Examiner's discussion regarding claim 6). However, in Figure 5 and at column 8, lines 40-55, Burns et al. merely shows and describes a diplexer filter 522 comprising a high pass and a low pass filter for separating a low power, high frequency downstream signal from a high power, low frequency upstream signal, neither of which is a difference

signal representing a difference between a first time interval and a second time interval. Also, at column 12, lines 14-24, Burns et al. merely discloses how a digital filter could be used to average, or filter, successive timestamps obtained from a headend. Clearly, this does not disclose filtering of a difference signal representing a difference between a first time interval and a second time interval, as presently claimed. Thus, it is respectfully submitted that Burns et al. does not teach, or even suggest, the presently claimed invention. Accordingly, it is respectfully submitted that claim 1 should be allowable.

At this point it should be noted that claim 1 has been amended to include some of the limitations of claim 6. Thus, no new search and/or consideration regarding these limitations should be required.

Claims 2-10 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-10 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 2 recites that the method further comprises delaying the first timestamp

by a first delay amount so as to measure the first time interval between the first timestamp and the second timestamp as determined by the first clock signal. It is respectfully submitted that Burns et al. does not teach, or even suggest, this claimed feature. Accordingly, it is respectfully submitted that claim 2 should be allowable. Also, claim 3 recites that the method further comprises delaying the first timestamp by a second delay amount so as to measure the second time interval between the first timestamp and the second timestamp as determined by the second clock signal. It is respectfully submitted that Burns et al. does not teach, or even suggest, this claimed feature. Accordingly, it is respectfully submitted that claim 3 should be allowable. Further, claim 4 recites that the first delay amount and the second delay amount are substantially equal delay amounts. It is respectfully submitted that Burns et al. does not teach, or even suggest, this claimed feature. Accordingly, it is respectfully submitted that claim 4 should be allowable. Additionally, claim 6 now recites that the step of filtering the difference signal comprises filtering the difference signal with a low pass filter such that the second clock signal is synchronized with the first clock signal based upon the filtered difference signal. It is respectfully submitted that Burns et al. does not teach, or even suggest,

this claimed feature. Accordingly, it is respectfully submitted that claim 6 should be allowable. Regarding claims 5 and 7-10, Applicants would like to remind the Examiner that, as stated in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

Regarding claim 20, the same arguments apply as set forth above with respect to claim 1.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-10 and 20 be withdrawn.

II. THE OBVIOUSNESS REJECTION OF CLAIMS 11-19

On pages 7-10 of the Office Action, claims 11-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Burns et al. (U.S. Patent No. 6,449,291) in view of Rokugo (U.S.

Patent No. 5,864,248). This rejection is hereby respectfully traversed with amendment.

Under 35 U.S.C. § 103, the Patent Office bears the burden of establishing a prima facie case of obviousness. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). The Patent Office can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of references. Id. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). That is, under 35 U.S.C. § 103, teachings of references can be combined only if there is some suggestion or motivation to do so. Id. However, the motivation cannot come from the applicant's invention itself. In re Oetiker, 977 F.2d 1443, 1447, 24 USPQ2d 1443, 1446 (Fed. Cir. 1992). Rather, there must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the art would make the combination. Id.

Regarding claim 11, the Examiner asserts that Burns et al. discloses: a receiver for receiving a first timestamp and a

second timestamp each indicating a respective time instance within the network; a first differencing element for measuring a first time interval between the first timestamp and the second timestamp as determined by a first clock signal; a second differencing element for measuring a second time interval between the first timestamp and the second timestamp as determined by a second clock signal; a third differencing element for generating a difference signal representing a difference between the first time interval and the second time interval; and a variable oscillator for generating the second clock signal based upon the difference signal such that the second clock signal is synchronized with the first clock signal. The Examiner acknowledges that Burns et al. fails to disclose a phase-locked loop associated with a receiver. The Examiner then goes on to assert that Rokugo discloses a phase-locked loop associated with a receiver, and thus it would have been obvious to combine the teachings of Burns et al. and Rokugo so as to arrive at the claimed invention.

However, it is respectfully submitted that Burns et al. and Rokugo, either alone or in combination, fail to teach, or even suggest, an apparatus for synchronizing clocks in a network comprising: a receiver for receiving a first timestamp and a second timestamp each indicating a respective time instance

within the network; and a phase-locked loop associated with the receiver, the phase-locked loop comprising: a first differencing element for measuring a first time interval between the first timestamp and the second timestamp as determined by a first clock signal; a second differencing element for measuring a second time interval between the first timestamp and the second timestamp as determined by a second clock signal; a third differencing element for generating a difference signal representing a difference between the first time interval and the second time interval; a filter for filtering the difference signal; and a variable oscillator for generating the second clock signal based upon the filtered difference signal such that the second clock signal is synchronized with the first clock signal, as presently claimed. Indeed, neither Burns et al. nor Rokugo disclose, or even suggest, either alone or in combination, anything regarding the filtering of a difference signal representing a difference between a first time interval and a second time interval. Despite this deficiency, the Examiner asserts that Burns et al. does disclose filtering of a difference signal in Figure 5, at column 8, lines 40-55, and column 12, lines 14-24 (see Examiner's discussion regarding claim 6). However, in Figure 5 and at column 8, lines 40-55, Burns et al. merely shows and describes a diplexer filter 522

comprising a high pass and a low pass filter for separating a low power, high frequency downstream signal from a high power, low frequency upstream signal, neither of which is a difference signal representing a difference between a first time interval and a second time interval. Also, at column 12, lines 14-24, Burns et al. merely discloses how a digital filter could be used to average, or filter, successive timestamps obtained from a headend. Clearly, this does not disclose filtering of a difference signal representing a difference between a first time interval and a second time interval, as presently claimed. Rokugo also does not disclose, or even suggest, filtering of a difference signal representing a difference between a first time interval and a second time interval. Thus, it is respectfully submitted that Burns et al. and Rokugo, either alone or in combination, do not disclose, or even suggest, the presently claimed invention. Accordingly, it is respectfully submitted that claim 11 should be allowable.

At this point it should be noted that claim 11 has been amended to include some of the limitations of claim 16. Thus, no new search and/or consideration regarding these limitations should be required.

Claims 12-19 are dependent upon independent claim 11. Thus, since independent claim 11 should be allowable as

discussed above, claims 12-19 should also be allowable at least by virtue of their dependency on independent claim 11. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 12 recites that the apparatus further comprises a first delay element for delaying the first timestamp by a first delay amount so as to measure the first time interval between the first timestamp and the second timestamp as determined by the first clock signal. It is respectfully submitted that Burns et al. and Rokugo, either alone or in a combination, do not teach, or even suggest, this claimed feature. Accordingly, it is respectfully submitted that claim 12 should be allowable. Also, claim 13 recites that the apparatus further comprises a second delay element for delaying the first timestamp by a second delay amount so as to measure the second time interval between the first timestamp and the second timestamp as determined by the second clock signal. It is respectfully submitted that Burns et al. and Rokugo, either alone or in a combination, do not teach, or even suggest, this claimed feature. Accordingly, it is respectfully submitted that claim 13 should be allowable. Further, claim 14 recites that the first delay amount and the second delay amount are substantially equal delay amounts. It

is respectfully submitted that Burns et al. and Rokugo, either alone or in a combination, do not teach, or even suggest, this claimed feature. Accordingly, it is respectfully submitted that claim 14 should be allowable. Additionally, claim 16 now recites that the filter comprises a low pass loop filter for filtering the difference signal such that the second clock signal is synchronized with the first clock signal based upon the filtered difference signal. It is respectfully submitted that Burns et al. and Rokugo, either alone or in a combination, do not teach, or even suggest, this claimed feature. Accordingly, it is respectfully submitted that claim 16 should be allowable. Regarding claims 15 and 17-19, Applicants would like to remind the Examiner that, as stated in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 11-19 be withdrawn.

III. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

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APPENDIX A

1 (Currently Amended). A method for synchronizing clocks in a network, the method comprising the steps of:

receiving a first timestamp and a second timestamp each indicating a respective time instance within the network;

measuring a first time interval between the first timestamp and the second timestamp as determined by a first clock signal;

measuring a second time interval between the first timestamp and the second timestamp as determined by a second clock signal;

generating a difference signal representing a difference between the first time interval and the second time interval;

filtering the difference signal; and

generating the second clock signal based upon the filtered difference signal such that the second clock signal is synchronized with the first clock signal.

2 (Previously Presented). The method as defined in claim 1, further comprising the step of:

delaying the first timestamp by a first delay amount so as to measure the first time interval between the first timestamp and the second timestamp as determined by the first clock signal.

3 (Previously Presented). The method as defined in claim 2, further comprising the step of:

delaying the first timestamp by a second delay amount so as to measure the second time interval between the first timestamp and the second timestamp as determined by the second clock signal.

4 (Previously Presented). The method as defined in claim 3, wherein the first delay amount and the second delay amount are substantially equal delay amounts.

5 (Original). The method as defined in claim 1, further comprising the step of:

initializing the difference signal prior to receiving the first timestamp and the second timestamp.

6 (Currently Amended). The method as defined in claim 1, wherein the step of filtering the difference signal ~~further comprising the step of:~~

~~comprises~~ comprises filtering the difference signal with a low pass filter such that the second clock signal is synchronized with the first clock signal based upon a the filtered difference

signal.

7 (Original). The method as defined in claim 6, further comprising the step of:

initializing the filtered difference signal prior to receiving the first timestamp and the second timestamp.

8 (Currently Amended). The method as defined in claim 1, wherein the step of generating the second clock signal comprises the step of:

controlling the period of a digitally controlled oscillator based upon the filtered difference signal.

9 (Currently Amended). The method as defined in claim 1, wherein the step of generating the second clock signal comprises the step of:

converting the filtered difference signal from a digital difference signal value into an analog difference signal value; and

controlling the period of a voltage controlled oscillator based upon the analog difference signal value.

10 (Original) A computer signal embodied in a carrier wave

readable by a computing system and encoding a computer program of instructions for executing a computer process performing the method recited in claim 1.

11 (Currently Amended). An apparatus for synchronizing clocks in a network, the apparatus comprising:

a receiver for receiving a first timestamp and a second timestamp each indicating a respective time instance within the network; and

a phase-locked loop associated with the receiver, the phase-locked loop comprising:

a first differencing element for measuring a first time interval between the first timestamp and the second timestamp as determined by a first clock signal;

a second differencing element for measuring a second time interval between the first timestamp and the second timestamp as determined by a second clock signal;

a third differencing element for generating a difference signal representing a difference between the first time interval and the second time interval;

a filter for filtering the difference signal; and

a variable oscillator for generating the second clock signal based upon the filtered difference signal such that the

second clock signal is synchronized with the first clock signal.

12 (Previously Presented). The apparatus as defined in claim 11, further comprising:

a first delay element for delaying the first timestamp by a first delay amount so as to measure the first time interval between the first timestamp and the second timestamp as determined by the first clock signal.

13 (Previously Presented). The apparatus as defined in claim 12, further comprising:

a second delay element for delaying the first timestamp by a second delay amount so as to measure the second time interval between the first timestamp and the second timestamp as determined by the second clock signal.

14 (Previously Presented). The apparatus as defined in claim 13, wherein the first delay amount and the second delay amount are substantially equal delay amounts.

15 (Original). The apparatus as defined in claim 11, wherein the second differencing element initializes the difference signal prior to receiving the first timestamp and the second timestamp.

16 (Currently Amended). The apparatus as defined in claim 11, wherein the filter comprises ~~further comprising:~~
——a low pass loop filter for filtering the difference signal such that the second clock signal is synchronized with the first clock signal based upon a the filtered difference signal.

17 (Original). The apparatus as defined in claim 16, wherein the loop filter initializes the filtered difference signal prior to receiving the first timestamp and the second timestamp.

18 (Currently Amended). The apparatus as defined in claim 11, wherein the variable oscillator is a digitally controlled oscillator the period of which is controlled based upon the filtered difference signal.

19 (Currently Amended). The apparatus as defined in claim 11, further comprising:

a digital-to-analog converter for converting the filtered difference signal from a digital difference signal value into an analog difference signal value, and wherein the variable oscillator is a voltage controlled oscillator the period of which is controlled based upon the analog difference signal

value.

20 (Currently Amended). An article of manufacture for synchronizing clocks in a network, the article of manufacture comprising:

at least one processor readable carrier; and

instructions carried on the at least one carrier;

wherein the instructions are configured to be readable from the at least one carrier by at least one processor and thereby cause the at least one processor to operate so as to:

receive a first timestamp and a second timestamp each indicating a respective time instance within the network;

measure a first time interval between the first timestamp and the second timestamp as determined by a first clock signal;

measure a second time interval between the first timestamp and the second timestamp as determined by a second clock signal;

generate a difference signal representing a difference between the first time interval and the second time interval;

filter the difference signal; and

generate the second clock signal based upon the filtered difference signal such that the second clock signal is synchronized with the first clock signal.